

# ICCDC 2019 LNEE SPRINGER

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**Abstract.** Reed Solomon codes are commonly used to detect and correct errors in digital data during transmission and storage. In this paper, a new optimization algorithm has been proposed which is very simple and efficient for reducing the complexity of the Galois field constant multipliers in terms of XOR2 gates and hence the area overhead of RS(32, 28) encoder decreases.

**Key words:** Compact disc and FPGA

## 1 Introduction

Existing optimization techniques are basically based on common sub-expression elimination methods [7]. These methods are very difficult to design RS codec for higher error correction capability. In this paper, We have proposed a new optimization algorithm which is

## 2 ABCD

**Table 1.** Complexity comparison of

Multipl. Constant	No. of XOR2 without opt.	No. of XOR2 using proposed local opt. algo	No. of XOR2 using proposed global opt. algo
Total	103	67	51
Improvement (%) over without opt.	-	34.95	50.49

$$g(x) = x^4 + 30x^3 + 216x^2 + 231x + 116 \quad (1)$$

## 3 CONCLUSION

In this paper, a new optimization algorithm has been proposed to design constant GF(2<sup>8</sup>) field multiplier. The proposed algorithm is very

